IN THE CLAIMS

1-11. (canceled)

12. (new) A vertical junction field-effect transistor (VJFET) having a plurality of semiconductor layers, comprising:

a drain layer of heavily doped semiconductor of a first conductivity type and operable as a drain for said transistor;

a blocking layer of lightly doped semiconductor of the first conductivity type formed on top of said drain layer;

a channel layer formed on top of said blocking layer; the channel layer having a plurality of vertical channels of the first conductivity type spaced apart by U-shaped regions of heavily doped semiconductor of the second conductivity type; the second conductivity type having an opposite conductivity of the first conductivity type; wherein the sides of the U-shaped regions form vertical gate junctions with said vertical channels; and

a source layer of very heavily doped semiconductor of the first conductivity type on top of said vertical gate junctions and operable as a source for said transistor;

wherein said vertical gate junctions produce a vertical channel opening of a uniform width for operation of the VJFET.

13. (new) The vertical junction field-effect transistor according to Claim 12, wherein the U-shaped regions are doped by angled ion implantation.

14. (new) The vertical junction field-effect transistor according to Claim 12, further comprising gate ohmic contacts to very heavily doped semiconductor of the second conductivity type formed on the inside bottom of the U-shaped regions.

15. (new) The vertical junction field-effect transistor according to Claim 14, further comprising passivation regions covering the sides of the U-shaped regions, at least part of the gate ohmic contacts, and the sides of the source layer on top of said vertical gate junctions.

16. (new) The vertical junction field-effect transistor according to Claim 15, further comprising a dielectric fill layer filling an area between the sides of the passivation regions.

17. (new) The vertical junction field-effect transistor according to Claim 12, further comprising a metal ohmic contact layer on top of the source layer.

18. (new) The vertical junction field-effect transistor according to Claim 12, wherein the VJFET is a normally-off transistor.

19. (new) The vertical junction field-effect transistor according to Claim 12, wherein the vertical gate junctions are perpendicular to said source layer to within twenty degrees (20°).

20. (new) The vertical junction field-effect transistor according to Claim 12, wherein an opening dimension of the vertical channel opening is uniform to within 0.3um.

21. (new) The vertical junction field-effect transistor according to Claim 12, wherein the vertical channel opening has a channel length (L_{vc}) between 0.5um and 3.5um.

22. (new) A vertical junction field-effect transistor (VJFET) having a plurality of semiconductor layers, comprising:

an n^+-type drain layer operable as a drain for said transistor;

an n^--type blocking layer formed on top of said drain layer;

a channel layer formed on top of said n^--type blocking layer; the channel layer having a plurality of vertical n-

type channels spaced apart by U-shaped p^+-type regions; wherein the sides of the U-shaped p^+-type regions form vertical p^+n gate junctions with said vertical n-type channels; and

an n^{++}-type source layer on top of said vertical p^+n gate junctions and operable as a source for said transistor;

wherein said vertical p^+n gate junctions are operable as a gate for said transistor and produce a vertical channel opening of a uniform width for operation of the VJFET.

23. (new) The vertical junction field-effect transistor according to Claim 22, wherein the U-shaped p^+-type regions are doped by angled ion implantation.

24. (new) The vertical junction field-effect transistor according to Claim 22, further comprising p^{++}-type gate ohmic contacts to the inside bottom of the U-shaped p^+-type regions.

25. (new) The vertical junction field-effect transistor according to Claim 24, further comprising passivation regions covering the sides of the U-shaped p^+-type regions, at least part of the p^{++}-type gate ohmic contacts, and the sides of the n^{++}-type source layer on top of said vertical p^+n gate junctions.

26. (new) The vertical junction field-effect transistor according to Claim 25, further comprising a dielectric fill layer filling an area between the sides of the passivation regions.

27. (new) The vertical junction field-effect transistor according to Claim 22, further comprising a metal ohmic contact layer on top of the n^{++}-type source layer.

28. (new) The vertical junction field-effect transistor according to Claim 22, wherein the VJFET is a normally-off transistor.

29. (new) The vertical junction field-effect transistor according to Claim 22, wherein the vertical $p^{+}n$ gate junctions are perpendicular to said source layer to within twenty degrees (20°).

30. (new) The vertical junction field-effect transistor according to Claim 22, wherein an opening dimension of the vertical channel opening is uniform to within 0.3um.

31. (new) The vertical junction field-effect transistor according to Claim 22, wherein the vertical channel opening has a channel length (L_{vc}) between 0.5um and 3.5um.